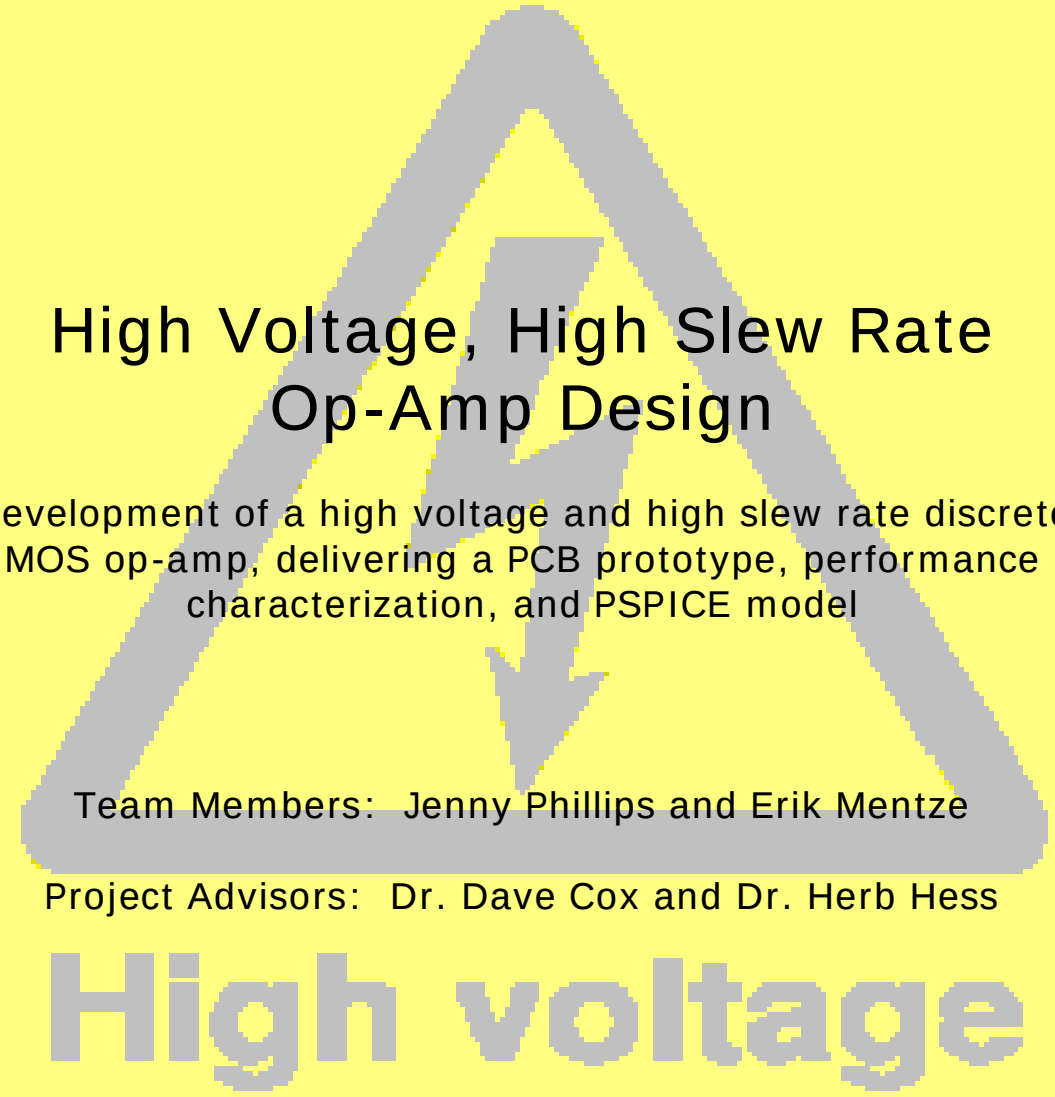
High Voltage, High Slew Rate Op-Amp Design

Development of a high voltage and high slew rate discrete MOS op-amp, delivering a PCB prototype, performance characterization, and PSPICE model

Team Members: Jenny Phillips and Erik Mentze

Project Advisors: Dr. Dave Cox and Dr. Herb Hess



Sponsor: Apex Microtechnology

April 24, 2005

Executive Summary:

The purpose of this project is to design and implement a high voltage (+/- 200V) operational amplifier with a high slew rate (at least 1000V/μs). While similar amplifiers have been successfully implemented in the past, our purpose is to achieve higher slew-rates than commonly reported and investigate new techniques to accomplish this.

This report highlights the advantages of a 3 stage, dual path amplifier as a general topology for successfully implementing our design goals. This topology was originally reported less than a year ago for low-voltage, integrated circuit applications. The advantage of this circuit topology is that it takes advantage of active frequency compensation techniques to use comparatively small compensation capacitors, while maintaining high gain and wide bandwidth. Further, in this report we present some of the specific gain stages being considered to implement this specific amplifier.

This report then discusses the specific implementation of the concepts discussed along with simulation results from PSPICE. The three-stage design works well for generating high slew rates and works at the 400 V differential level. The results include DC biasing information, power dissipation, and the waveforms generated. The phase margin is adequate for stability.

Finally, the report details the physical implementation including the PCB layout, discrete components chosen, and the test setup. The populated PCB is ready for testing when the necessary equipment is available. It is recommended that this design be implemented in the future in IC technology, as the concepts developed and simulation results indicate a successful design.

Table of Contents:

Background-

The operational amplifier has a variety of uses as a circuit component, including control, filtering, amplification, feedback, and regulation. It is a fundamental building block for many circuit designs that utilize its high gain, high input impedance, and low output impedance. As the world of electronics is scaled to smaller dimensions and power consumption is drastically reduced, research work has tended to focus on monolithic implementations of amplifiers whose differential power supply is only a few volts. Consequently many interesting new discoveries have been made for amplifiers that operate in the low-voltage range. However, there is still a need for their high-voltage discrete counterparts. Although little active research is being carried out in this area, many possibilities exist in taking advantage of advances in low-voltage amplifier design for developing high-voltage amplifiers.

One of the significant challenges that arise in low-voltage, fully integrated amplifier design is the sizing of the compensation capacitors. The most expensive real-estate in the world is the silicon on which microelectronics are built. It is not uncommon for the compensation capacitor used for a fully integrated amplifier to populate almost as much space as the amplifier itself. Because of this, a significant amount of effort goes into minimizing the capacitor size. In designing a high slew-rate amplifier, we also need to minimize the size of the compensation capacitor, but for an entirely different reason. Slew-rate is inversely proportional to the compensation capacitor size. By reducing its size we increase the slew-rate. As such, we can capitalize on current research in the area of reducing capacitor sizing.

Currently Apex Microtechnology offers many discrete operational amplifiers for power applications, including test and measurement, industrial control, and aerospace/military. However, for +/- 200V power supplies, the maximum slew rate they have listed is 170 V/µs. Through this project we are attempting to extend this current product offering, achieve a high-voltage amplifier design that has a far greater slew rate (1000 V/µs).

Problem Definition-

This project centers around the design of a high voltage, high slew rate operational amplifier. The operating voltage is +/- 200V (400V differential) and the slew rate required is 1000 V/µs. All other operational parameters are variable. However, considerations such as gain, bandwidth, output drive current, and power dissipation must be taken into account to ensure the usefulness of the end product. Since these are flexible parameters we are able to use them in design tradeoffs, and they do not take precedence over the voltage and slew rate specifications.

The end deliverables will be the final design of the operational amplifier described above. This will be fully tested using PSPICE simulations. The prototype will be a PCB implementation of the design using discrete MOSFETs. Using discrete components to prototype the amplifier design is primarily conceptual since the device mismatch will lead to a significant reduction in performance.

Concept Development-

- General Topology:

The three stage, dual path topology presented in Figure 1 offers an elegant method of increasing the slew rate. The general topology utilizes two signal paths and active feedback frequency compensation. The active compensation is comprised of two segments: the damping-factor control block and the active-capacitive feedback network. The damping-factor control block, represented as gm4 and Cb in Figure 1, controls the non-dominate pole, while the active-capacitive feedback network, shown as gma and Ca in Figure 1, controls the 3dB, or dominate, pole. The governing equations can be found in Appendix A.

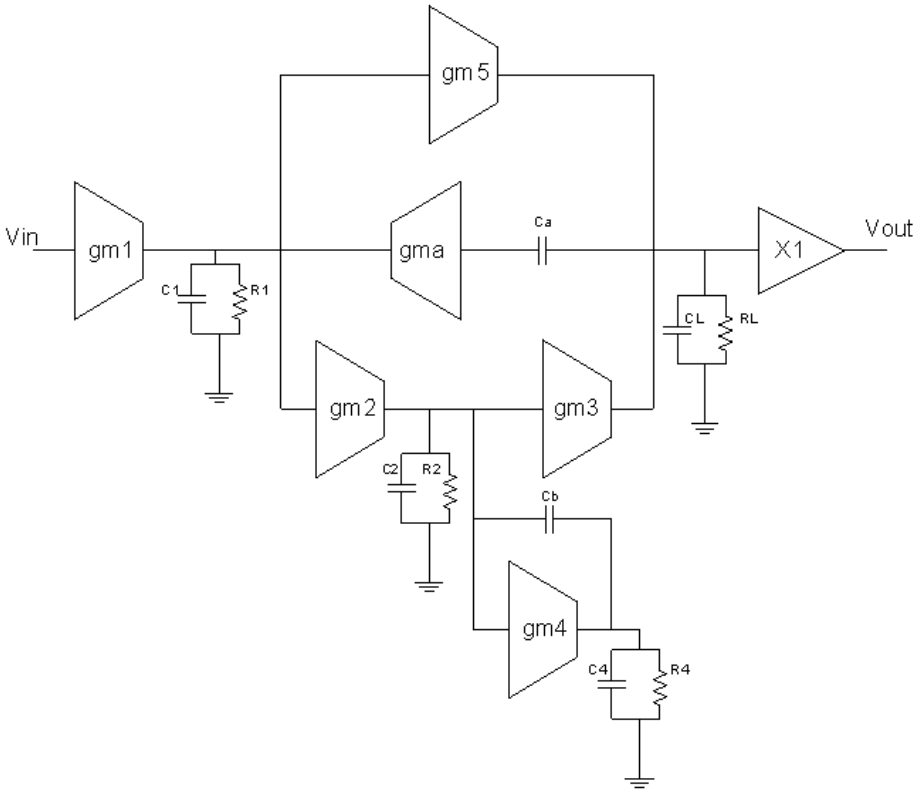


Figure 1: Three-Stage, Dual Path Amplifier Topology

In high slew rate amplifier design a two stage topology is typically used. This approach does have the advantage of simplicity. However, the three stage amplifier has extended bandwidth, smaller compensating capacitances, and allows one to independently size gain stages that drive capacitors. The active feedback allows the frequency and phase response of the amplifier to be modeled after any frequency response, such as a Butterworth response, which will give wide bandwidth and good phase margin. Table 1 below presents a comparative summary of the sizing of the compensation capacitors for the two and three stage amplifiers. It can be seen that each portion contributing to the compensation capacitor's size is smaller for the three stage versus the standard two stage amplifier topology. These derivations can also be viewed in Appendix A.

Table 1: Stage Amplifier Topology Comparisons

2 Stage	**3 Stage**
Twice the arithmetic mean of the capacitances	The geometric mean of the capacitances
The ratio of the transconductances	The root of the ratio of the transconductances
Constant equal to one	Constant less than one

- Input Differential Amplifier Stage (gm1):

We chose the bias cross-coupled differential pair, shown in Figure 2, as the input stage. This is an unsaturated differential pair, which is important for the input stage since it lacks current limitations thus leading to improved slew rate.

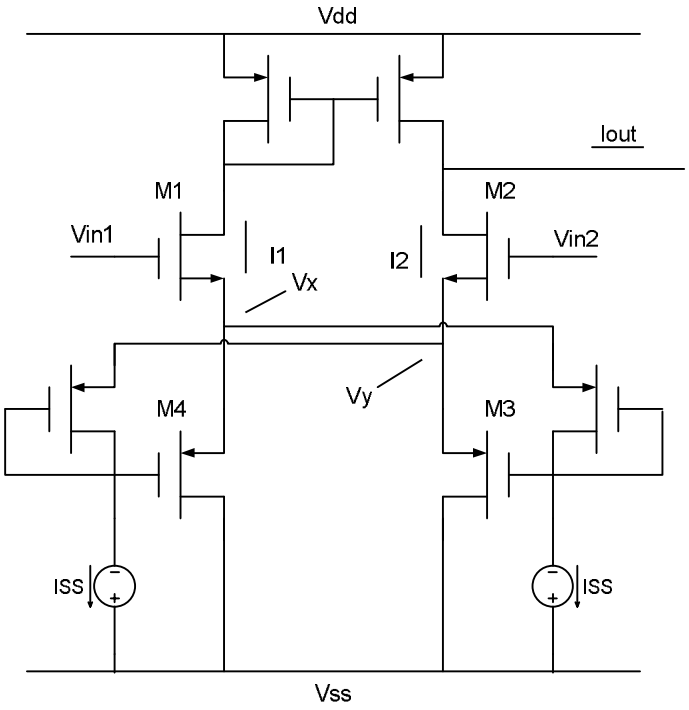

Vdd
Iout
M1
M2
Vin1
I1
I2
Vin2
Vx
Vy
M4
M3
ISS
ISS
Vss

Table 2: Unsaturated Differential Input Comparisons

Source Cross-Coupled	**Bias Cross-Coupled**
Off-Center Common Mode Range	Centered Common Mode Range
2 Gate Input Capacitances	1 Gate Input Capacitance
10 FETs	8 FETs
ID1 or ID2 equals zero for large inputs	ID1 and ID2 never equal zero
$GM = \frac{\partial(ID1 - ID2)}{\partial Vd} = \sqrt{2 \cdot ID \cdot b}$	$GM = \frac{\partial(ID1 - ID2)}{\partial Vd} = \frac{\sqrt{2}}{1+\sqrt{2}} \cdot \sqrt{2 \cdot ID \cdot b}$

- Intermediate Gain Stages (gm2, gm3, gm5):

The design of the intermediate stages began at the output. A Class AB, source follower, output stage was chosen because it will allow for the largest possible load and doesn't exhibit slew-rate limitations. Figure 3 contains the output stage. M23 and M24 set up the source-follower. A possible modification is to add a current limiting scheme that will keep all the transistors within their safe operating range. This is accomplished with the addition of a transistor and resistor on either side of the output node. Figure 3 has that modification added to it with M22 and M25.

Figure 3 incorporates two common-source amplifiers: M20, M27. These correspond to gm3 and gm5 respectively. Not shown in Figure 3 is gm2. This is another common-source amplifier that feeds directly into the gate of gm3. In implementation these common-source amplifiers take the form of common-source amplifiers with source degeneration. By adding degenerating resistors we are able to set the operating point of the amplifier more precisely.

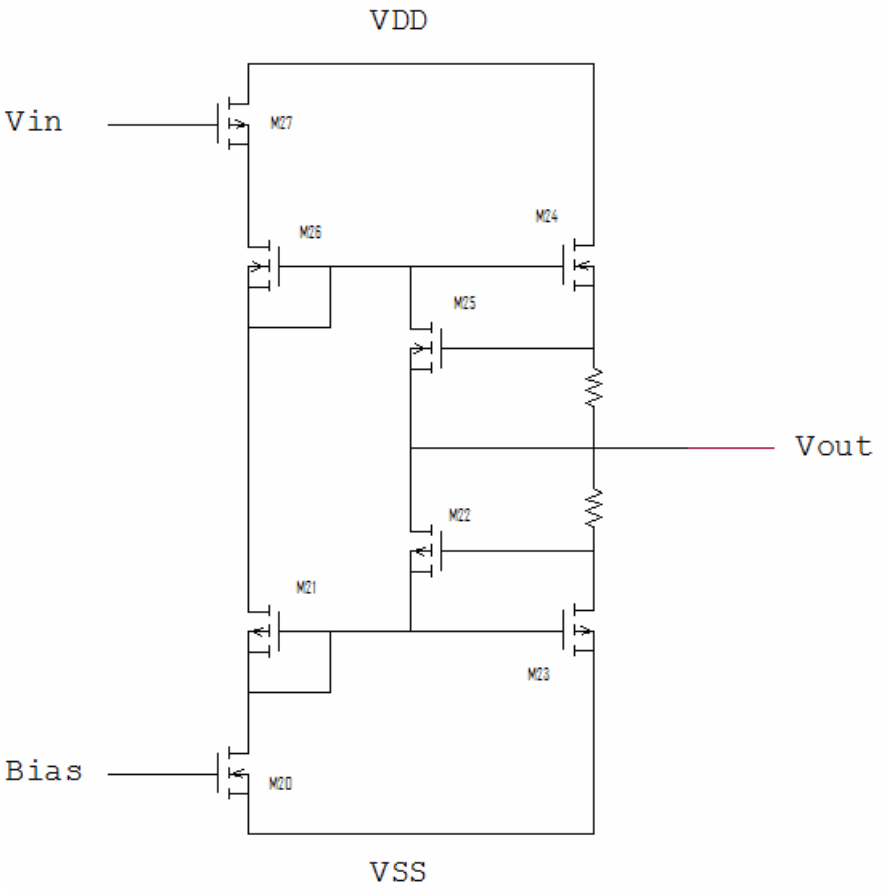


Figure 3: AB output with current limiting scheme

Product Description-

The general topology was implemented using the gain stages described above. The final circuit schematic with these gain stages is shown in Figure 4. Gma, the active frequency compensation gain stage, is implemented as a common-gate amplifier. Gm4 is not shown in Figure 4. The reason for this will be further explained later in this report.

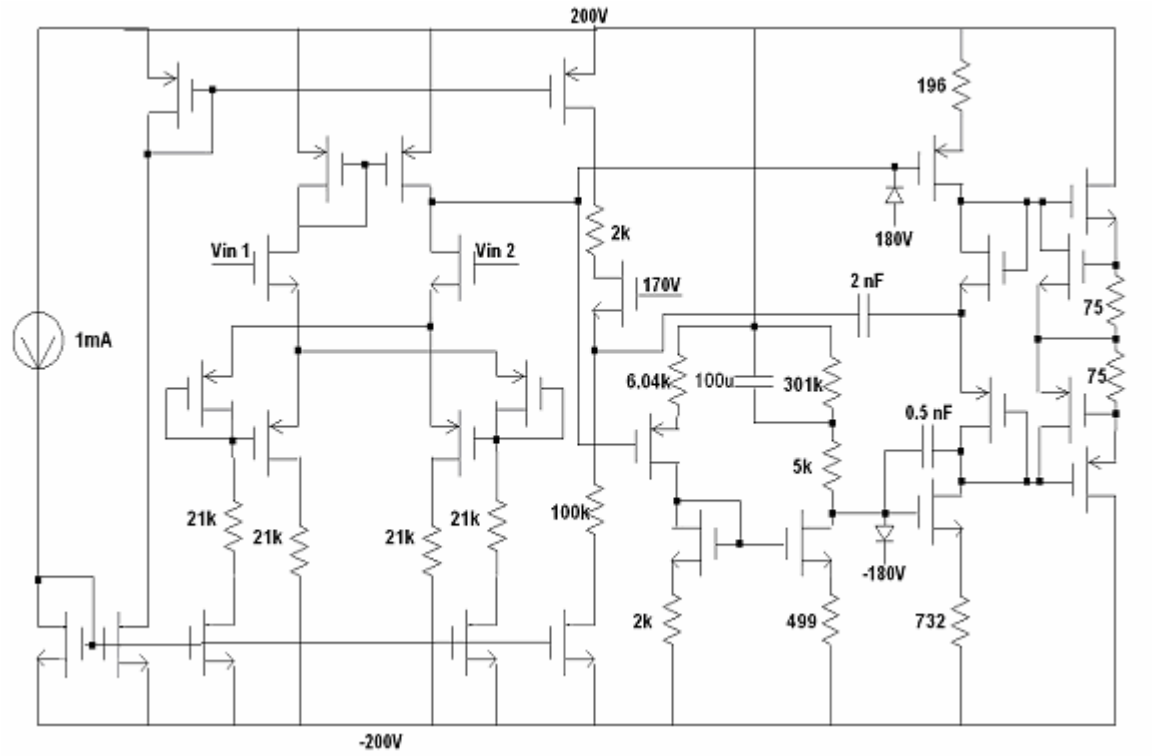


Figure 4: Full Circuit Schematic

The dual path topology, with the individual sub-circuits shown above, performs extremely well. The input stage exhibits extremely high slew rates and, as expected, does not have any current limitations (other than the individual device limitation). This input stage is a success and shows promise for being a good alternative to the cross-coupled differential amplifier that is typically used. The overall gain of the amplifier is very high, exceeding 110 dB.

Almost all components used have very low power dissipation. All transistors are under the limit of 750 mW, and only 2 resistors dissipate more than 500 mW. The two resistors that dissipated the most power are the two 21 kΩ resistors in the center of the input diff-amp. These resistors have almost the full 400 V across each of them while the input stage was driving large amounts of current.

Precision biasing is important to ensure that none of the transistors in the circuit exceed their power dissipation limit. Along with this careful biasing scheme, diodes, connected to external bias voltages, are used to restrict the two most sensitive nodes.

A 2 nF compensation capacitor is used in the active frequency compensation network. The second compensating capacitor, .5nF, is a Nested Miller Capacitor (NMC). This was used instead of the damping-factor control block prescribed by the dual-path topology. This change was made because of a lack of understanding of how that block should work, and a lack of information available on it in current published literature. To simplify the design at this point we chose to insert an NMC. This will restrict the amplifiers slew-rate in the high-to-low transition, but is a reasonable trade-off at this stage of prototyping the amplifier concept.

The PCB layout is shown in Figure 5. It is a two layer board ordered from PCB Express.

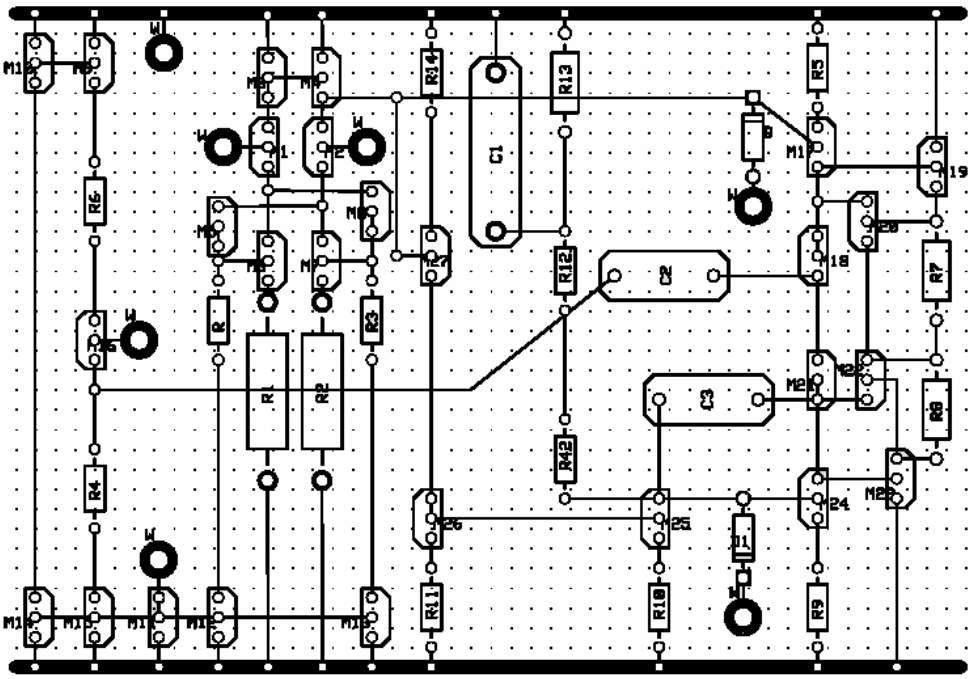


Figure 5: PCB Layout

This board was populated using the necessary transistors, resistors, capacitors, and diodes. These components were chosen on their ability to handle 400V and based on the required power dissipation for that specific part based on simulations. Complete descriptions of components used can be found in Appendix C.

Product Evaluation-

- DC Biasing

A famous analog circuit designer once said, "Biasing is 75% of circuit design, only 25% is signal path." This is referring to the importance of proper DC biasing. As such, we have taken great care in determining the proper DC operating points for this amplifier. The final configuration was simulated in PSPICE. Below, in Figure 6, the most important biasing voltages are shown.

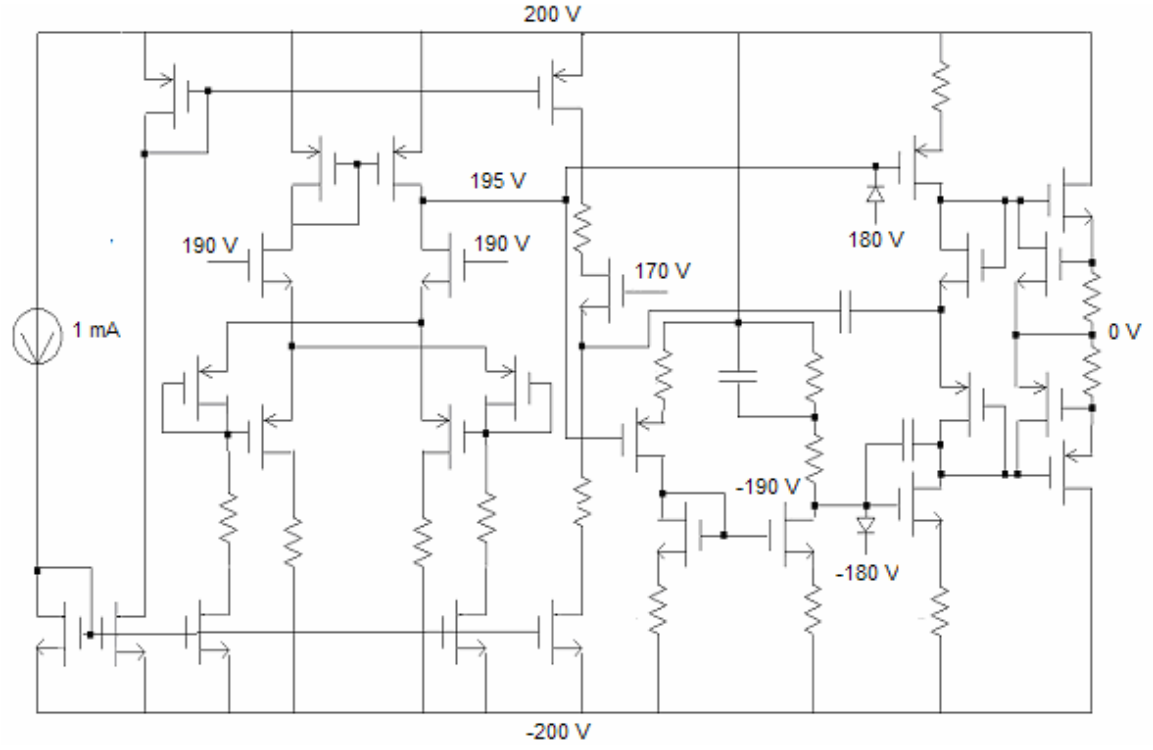


Figure 6: DC Biasing Voltages.

These operating points allow for maximum signal-swing while keeping any part in the circuit from exceeding its power dissipation limit. For the transistors, this limit was 750 mW. The power dissipation of the individual circuit elements is listed below in Table 3. The notation used in the table is illustrated below in Figure 7.

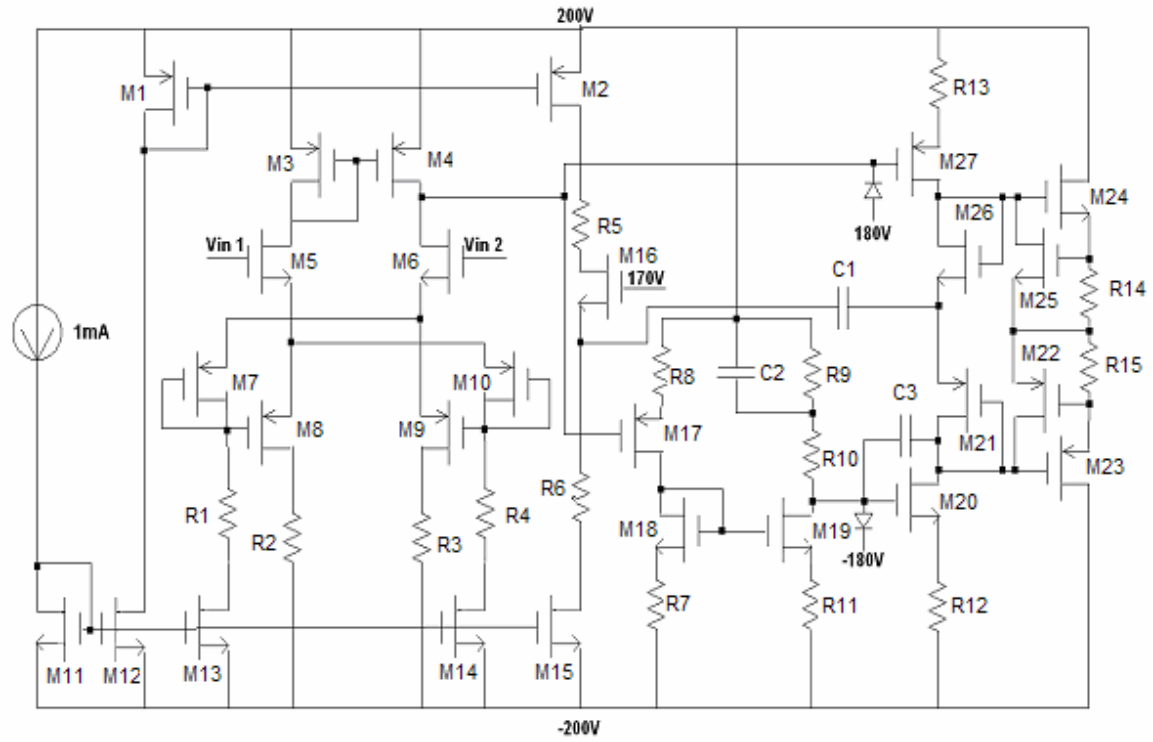


Figure 7: Static Power Dissipation.

Table3: Listing of Static Power Dissipation

Component	Power Dissipation [mW]	Component	Power Dissipation [mW]
M1	2.729	M15	268
M2	3.021	M16	27.24
M3	8.722	M17	157.1
M4	8.34	M18	.836
M5	28.68	M19	11.66
M6	22.37	M20	2.12
M7	2.728	M21	32
M8	700.9	M22	400
M9	708.6	M23	734.8
M10	2.728	M24	597.5
M11	3.2	M25	400
M12	2.2	M26	24.62
M13	364	M27	1.76
M14	364		

- Transient Operation

Figure 8 shows the transient operation of the amplifier under slewing conditions. This figure shows the +/- 200 volt rail-to-rail operation of the amplifier as well as the high slew-rate. Uncompensated, we achieved a rising slew-rate of 2000V/μs and a falling slew-rate of 700 V/μs. This asymmetry in slew-rates is a function of the asymmetry in the circuit. Because of the added gain stage in the lower signal path, the slew-rate for the transition from high-to-low is significantly slower than the slew-rate from low-to-high.

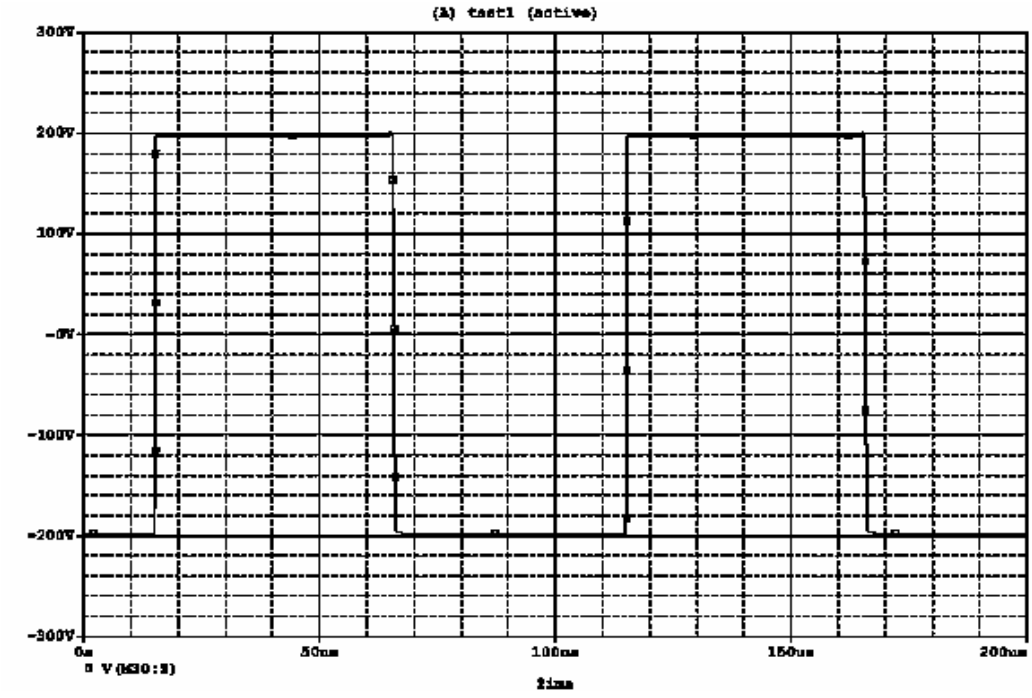


Figure 8: Slew Rate Simulations

- AC Operation

Because this circuit is a three stage amplifier, the gain is extremely high. As is shown in Figure 9, the DC gain is almost 120dB and the unity-gain frequency is over 100MHz.

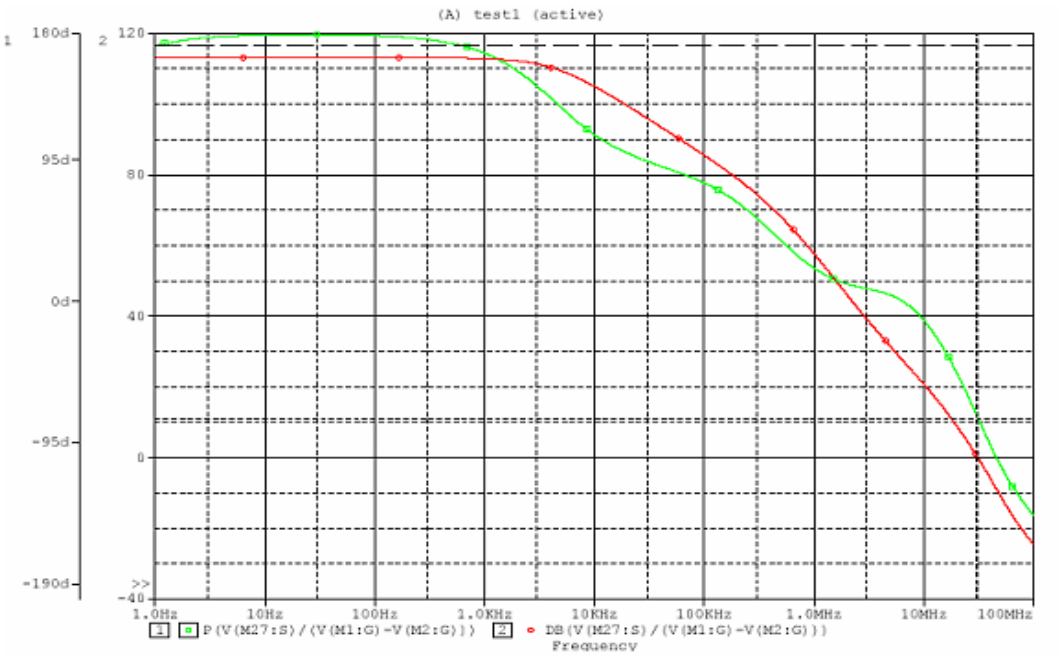


Figure 9: Uncompensated Gain Simulations

In compensating the amplifier, gain was sacrificed for phase margin. To achieve 35° of phase margin the above simulated capacitor sizes of 2nF and .5nF had to be used. This results in the frequency characteristic shown below in Figure 10. The DC gain is closer to 110dB and the unity-gain-frequency is over 10 MHz.

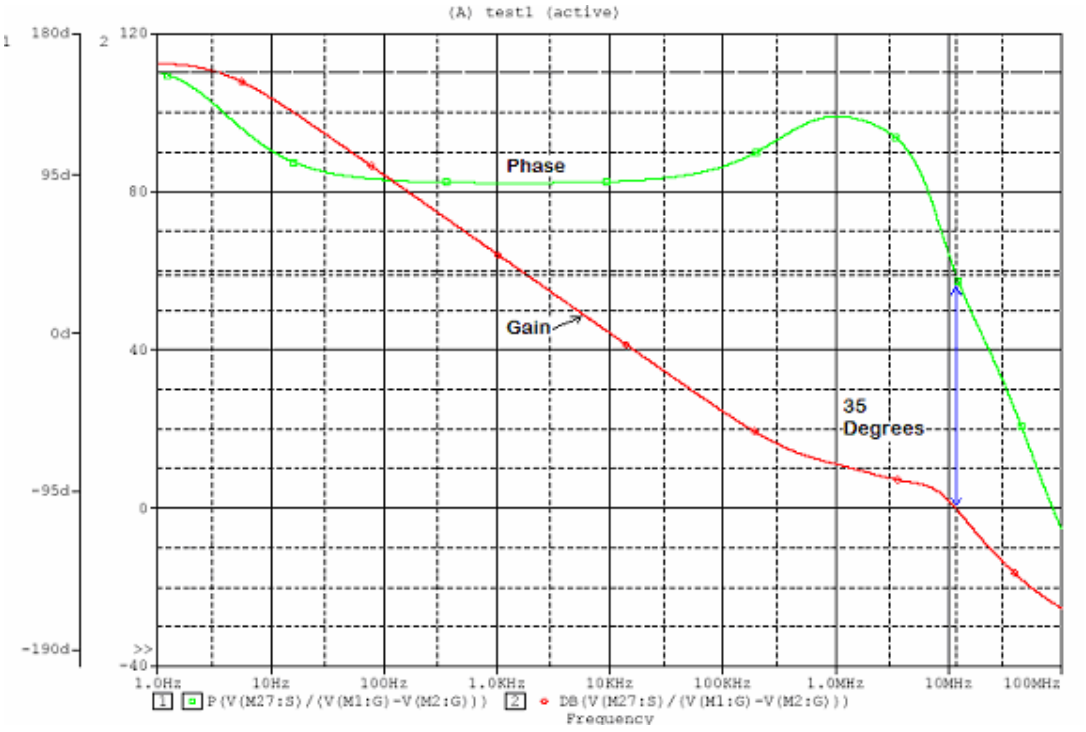


Figure 10: Compensated Gain Simulations

Overall, these simulation results show that this circuit meets the basic criteria of slew rate and voltage levels. The gain and bandwidth we achieved are as good as or better than many of the high slew rate amplifiers offered on the market today.

In implementing this design we ordered two PCB boards. One of the boards that came back had a short between two of its traces and was unusable. We populated the second board, including attaching banana plugs to the required locations on the board for measurement and biasing. The two high power-dissipating resistors were configured out of two, 10 kΩ resistors and one, 1 kΩ resistor, due to the lack of part availability within the time frame. These resistors were placed off the board. We created a test setup on perf-board with resistors to set up the DC biasing levels. We included potentiometers to fine-tune these levels once the entire setup was complete. Additionally we obtained a

special high-voltage power supply to test the design, but unfortunately it was not able to generate enough current to operate the amplifier. It is limited at 32 mA. The PCB with the amplifier and the biasing board are all set up and ready for testing when appropriate equipment is available. Pictures of the test setup can be seen in Appendix D.

Economic Considerations-

This project fell within the budget of $1000. The itemized costs can be seen in Table 3. We also had a power supply purchased through a separate fund for testing purposes.

Table 3: Cost Breakdown

Item	Total Cost
Transistors	$268.78
Resistors	$62.17
Resistors (High Power)	$103.32
Capacitors	$39.75
Diodes	$1.30
PCB Boards (2)	$104.55
Miscellaneous Test Equipment	$44.29
Total:	**$624.26**

Conclusions and Recommendations-

The general topology we used allowed dual signal pathways and active frequency compensation. We proved that most of the topology works, with the exception of the damping-factor control block, through the simulations. These simulations gave an excellent slew rate, which was a primary goal of the project. The topology was implemented with standard amplifiers for the individual gain blocks. The input stage

worked well in the design and appears to be a viable alternative to the source cross-coupled differential amplifier. The overall results of the simulation met the project specifications, including a higher slew rate than necessary on the rising edge. The falling edge slew rate could likely be improved if the damping-controlled block were to be successfully implemented. The physical setup is complete, including a fully populated PCB, though we will be unable to test this due to equipment constraints.

The other parameters of the operational amplifier are also acceptable: the design has good phase margin, gain, and bandwidth. The combination of the input stage and the individual gain blocks meant gain that easily exceeded 120 dB.

Overall, the topology is promising and offers a good methodology for high-voltage design in order to achieve high slew rate. This design exceeded expectations and it is likely that further work can further improve it, especially concentrated around the damping-factor control block. Due to device mismatch in discrete components, it is recommended that in the future the design be implemented in IC technology, or that surface mount devices and custom resistors are used.

Appendix A: General Amplifier Topologies and their Derivations

2- Stage Amplifier Analysis:

The 2 stage amplifier topology is straight forward and simple.

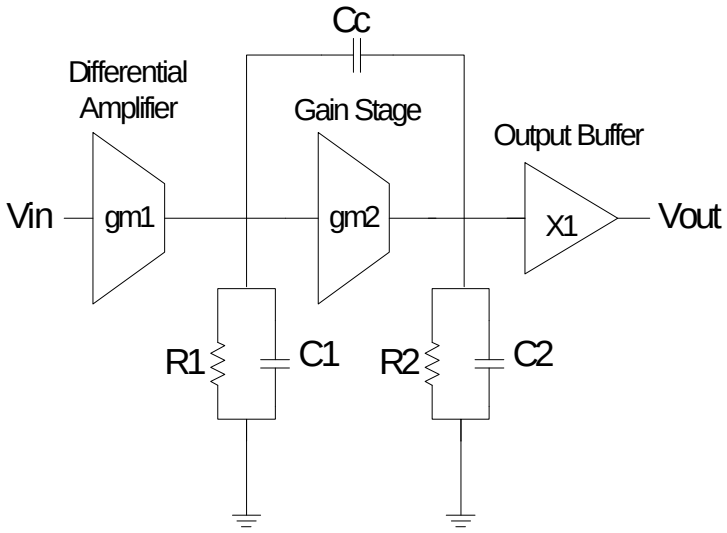


Figure A-1: 2-Stage Amplifier Topology

The governing equations follow.

The open loop gain is given by:

$$A_{OL} = A_1 \cdot A_2 = gm_1 \cdot gm_2 \cdot R_1 \cdot R_2$$

The pole locations can be found to be:

$$p_1 = \frac{1}{\left(1 + gm_2 \cdot R_2\right) \cdot C_c \cdot R_1} \qquad p_2 = \frac{gm_2 \cdot C_c}{C_2 \cdot C_1 + C_2 \cdot C_c + C_c \cdot C_1}$$

The compensation capacitor sizing is given by:

$$C_c = \left(\frac{gm_1}{gm_2}\right) \cdot \left(\frac{C_1 + C_2}{2}\right) + \sqrt{\left(\frac{gm_1}{gm_2}\right)^2 \cdot \left(\frac{C1 + C2}{2}\right)^2 + \left(\frac{gm_1}{gm_2}\right) \cdot \left(C_1 \cdot C_2\right)}$$

Cutting off the final term gives:

$$C_c > 2\left(\frac{gm_1}{gm_2}\right) \cdot \left(\frac{C_1 + C_2}{2}\right)$$

Three Stage, Dual Path Amplifier Analysis:

The three-stage, dual path amplifier is given below:

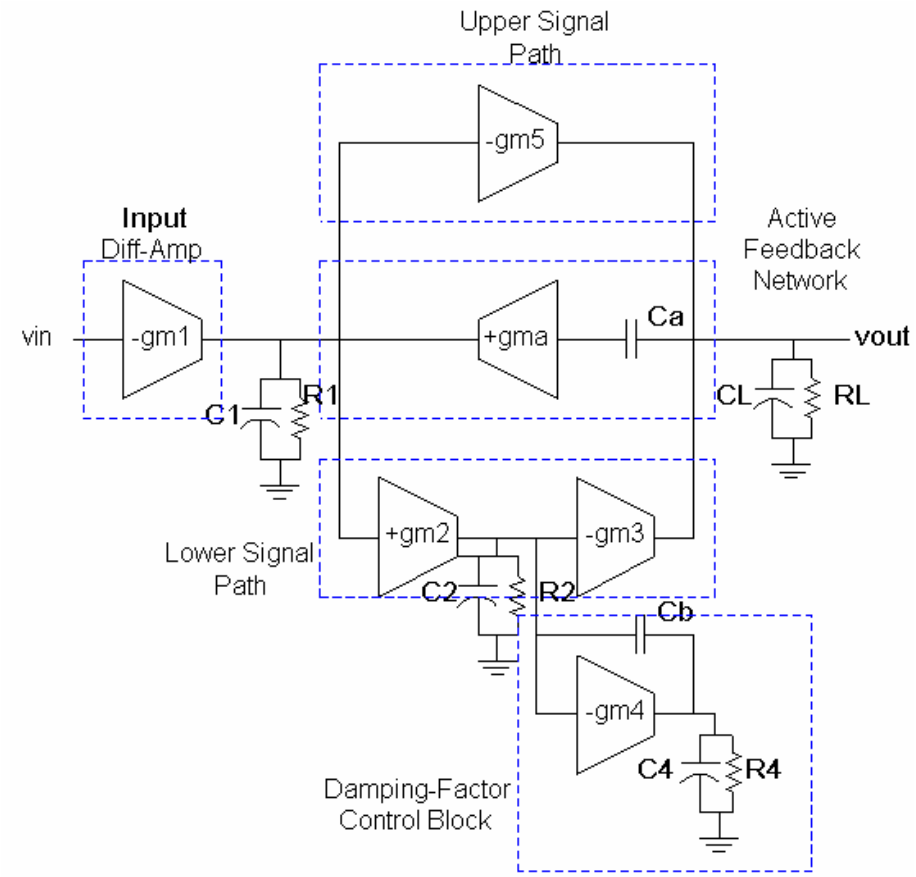


Figure A-2: 3 Stage, Dual Path Amplifier

The amplifier was modeled according to the Butterworth response:

$$B(s) = 1 + 2\left(\frac{s}{\omega_0}\right) + 2\left(\frac{s}{\omega_0}\right)^2 + \left(\frac{s}{\omega_0}\right)^3$$

This means that the active feedback transconductance stages and capacitors are set accordingly: $gm_a = 4gm1$

$$C_a = C_b = \sqrt{2 \cdot \left(\frac{gm_1 \cdot gm_4}{gm_2 \cdot gm_3 + gm_4 \cdot gm_5}\right) \cdot C_1 \cdot C_L}$$

The slew rate will be defined as:

$$SR = \min\left(\frac{I_b}{C_b}, \frac{I_a}{C_a}\right)$$

Where I_b and I_a are independently controllable currents available to charge and discharge the compensating capacitors. Setting *gm3=gm5* gives:

$$C_a = C_b = \sqrt{\frac{gm_1}{gm_{35}}} \cdot \sqrt{\frac{2}{1 + \frac{gm_2}{gm_4}}} \cdot \sqrt{C_1 \cdot C_L}$$

Appendix B: Unsaturated Differential Amplifier Analysis

The source cross-coupled diff pair and the bias cross-coupled diff pair can best be compared using a normalized approach, to eliminate variables not related to the topology. This is accomplished by assuming $V_{thP}=V_{thN}$ and $ß_N= ß_P=\mu C_{ox}(W/L)$.

Source Cross Coupled Analysis:

The source cross-coupled diagram is given below.

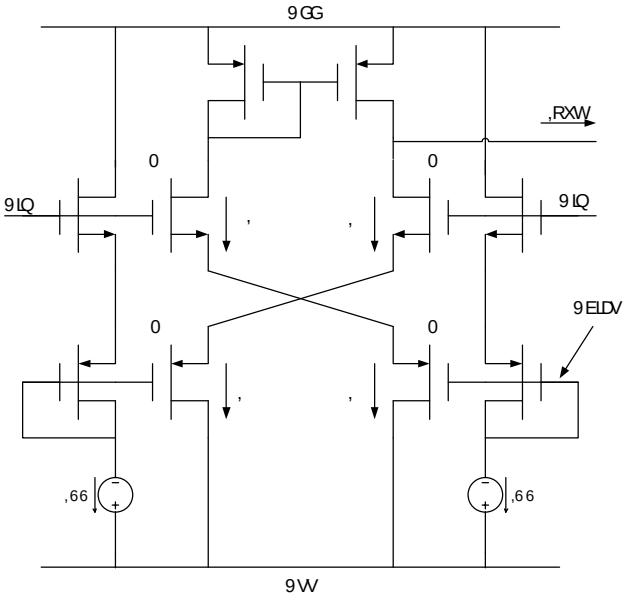


Figure B-1: Source Cross-Coupled Differential Amplifier

$$I_1 = \frac{b}{8}\left(V_{in1} + V_{bias} - 2V_{th}\right)^2$$

where: $V_{bias} = V_{GS(N)} + V_{SG(P)} = 2\sqrt{\frac{2I_{SS}}{b}} + 2V_{th}$

Substituting means that

$$\mathrm{I}_{\mathrm{D1}} = \frac{b}{8}\left(+ V_{Diff} + 2\sqrt{\frac{2I_{SS}}{b}}\right)^2$$

$$I_{D2} = \frac{b}{8}\left(-V_{Diff} + 2\sqrt{\frac{2I_{SS}}{b}}\right)^2$$

Considering the case when $V_{Diff} = 2\sqrt{\frac{2I_{SS}}{b}}$,

$$\frac{V_{Diff}}{V_{OV}} = 2 \text{ and } V_{OV} = \sqrt{\frac{2I_{SS}}{b}} = (V_{GS} - V_{th})$$

Considering when I_{D2}=0,

$$I_{D1} = \frac{b}{8}\left(2\sqrt{\frac{2I_{SS}}{b}} + 2\sqrt{\frac{2I_{SS}}{b}}\right)^2 = 4I_{SS} \text{ so that } \frac{I_{D1}}{I_{SS}} = 4$$

Bias Cross-Coupled Analysis:

Below is the schematic for the Bias Cross-Coupled Differential Amplifier.

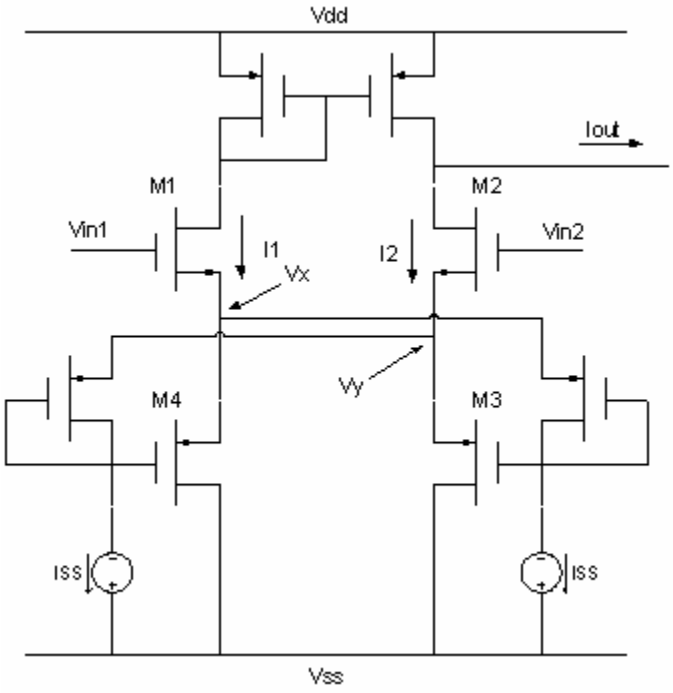


Figure B-2: Bias Cross-Coupled Schematic

It can be seen that $I_{D1} = I_{SS} + I_{D4}$

Further, $\frac{I_{D1}}{I_{SS}} = 1 + \frac{1}{2I_{SS}} b\left(V_x - V_y + \sqrt{\frac{2I_{SS}}{b}}\right)^2$ which leads to (after re-arranging),

$$\sqrt{\frac{b}{2I_{SS}}}\left(V_x - V_y\right) + 1 = \sqrt{\frac{I_{D1}}{I_{SS}} - 1}$$

Similar analysis for I_{D2} yields $\frac{I_{D2}}{I_{SS}} = 1 + \frac{1}{2I_{SS}} b\left(V_y - V_x + \sqrt{\frac{2I_{SS}}{b}}\right)^2$ and

$$\frac{I_{D2}}{I_{SS}} = 1 + \left(\sqrt{\frac{b}{2I_{SS}}}\left(V_y - V_x\right) + 1\right)^2$$

Substituting, $\frac{I_{D2}}{I_{SS}} = 1 + \left(2 - \sqrt{\frac{I_{D1}}{I_{SS}} - 1}\right)^2$

Bringing it all together,

$$V_{diff} = V_{in1} - V_{in2}$$

$$Vin1 = \sqrt{\frac{2I_{D1}}{b}} + V_x + V_{th}$$

$$Vin2 = \sqrt{\frac{2I_{D2}}{b}} + V_y + V_{th}$$

and finally

$$\frac{V_{diff}}{V_{OV}} = \sqrt{\frac{I_{D1}}{I_{SS}}} - \sqrt{\frac{I_{D2}}{I_{SS}}} + \left(\sqrt{\frac{I_{D1}}{I_{SS}} - 1} - 1\right)$$

This means that $1 \le \frac{I_{D1}}{I_{SS}} \le 5$ and $1 \le \frac{I_{D2}}{I_{SS}} \le 5$

So when $I_{D2} = I_{SS}$, $\frac{I_{D1}}{I_{SS}} = 5$ and $\frac{V_{diff}}{V_{OV}} = \sqrt{5}$

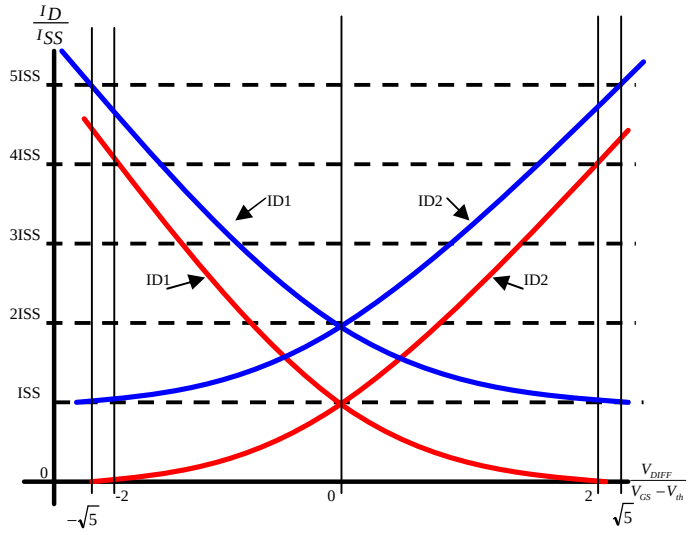


Figure B-3: Normalized drain current transfer characteristics for source cross-coupled and bias cross coupled differential amplifier. The dashed line is the source cross-coupled; the solid line is the bias cross-coupled.

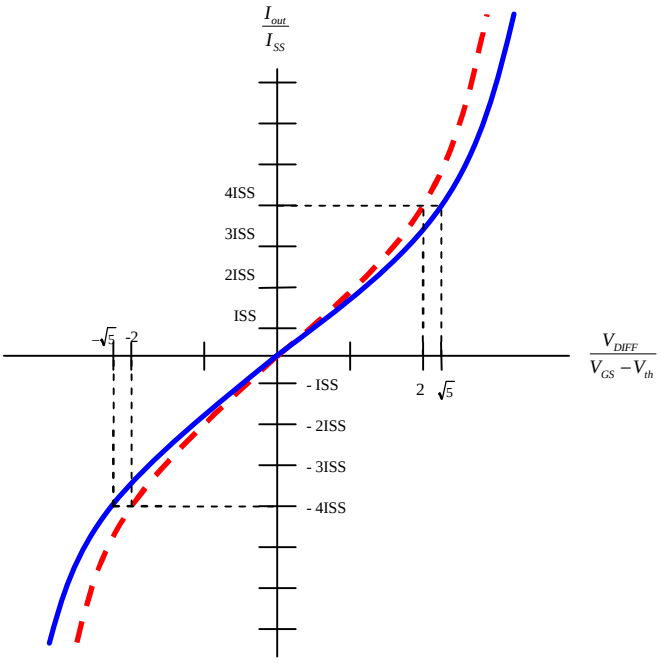


Figure B-4. Normalized output current transfer characteristics for source cross-coupled and bias cross coupled differential amplifier. The dashed line is the source cross-coupled; the solid line is the bias cross-coupled.

Appendix C: Discrete Parts Chosen

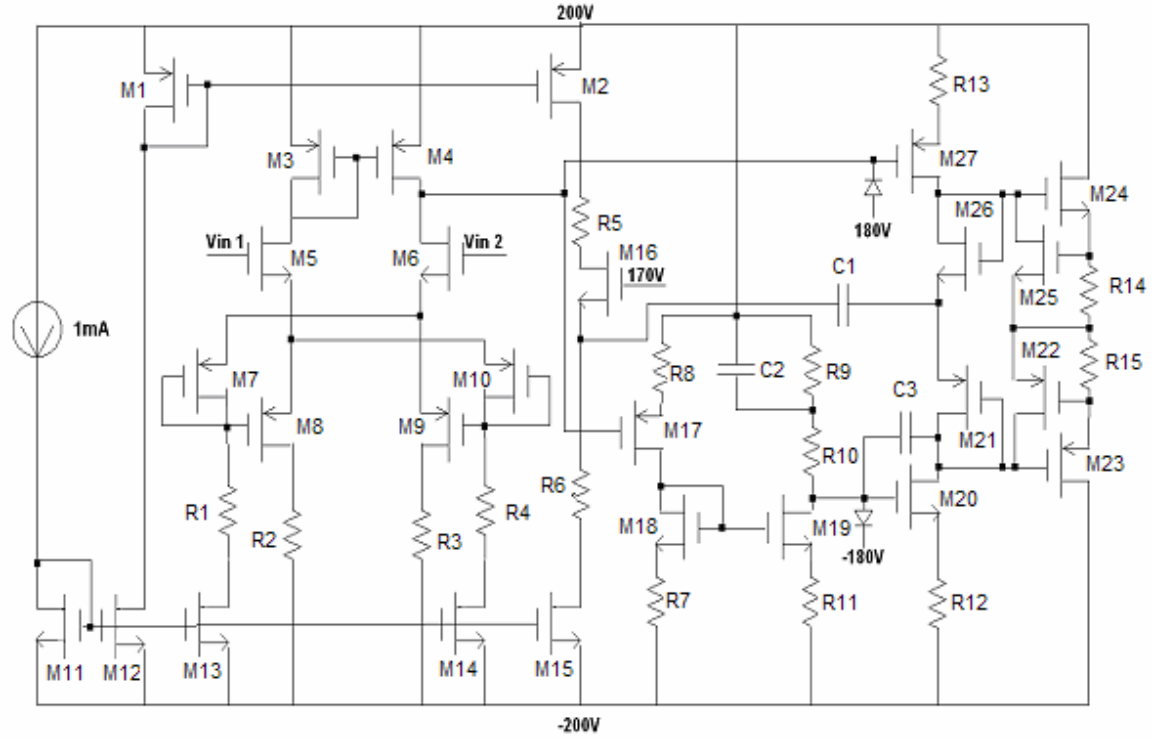


Figure C-1: Full Circuit Schematic

Transistors: ZVN0545A, ZVP0545A

Resistors:

- R1, R4: 66-RC55-D-21K (0.25 Watt)
- R2, R3: (2) 72-RCH5S-10K-1 and (1) 72-RCH5S-1K-1
- R5, R7: 66-RC55-D-2.0K (0.25 Watt)
- R6: 66-RC55-D-100K (0.25 Watt)
- R8: 66-RC55-D-6.04K (0.25 Watt)
- R9: 660-MF1/2CL10003F (0.5 Watt)
- R10: 66-RC55-D-4.99K and 66-RC55-D-10 (0.25 Watt)
- R11: 66-RC55-D-499 (0.25 Watt)
- R12: 66-RC55-D-732 (0.25 Watt)
- R13: 66-RC55-D-196 (0.25 Watt)
- R14, R15: 660-MF1/2CL75ROF (0.5 Watt)

Capacitors:

- C1: 2000 pF at 500V Mica
- C2: 100 mfd at 450 Volts Axial E-Cap
- C3: 500 pF at 500V Mica

Diodes: 625-1N5711

Appendix D: Physical Implementation Setup

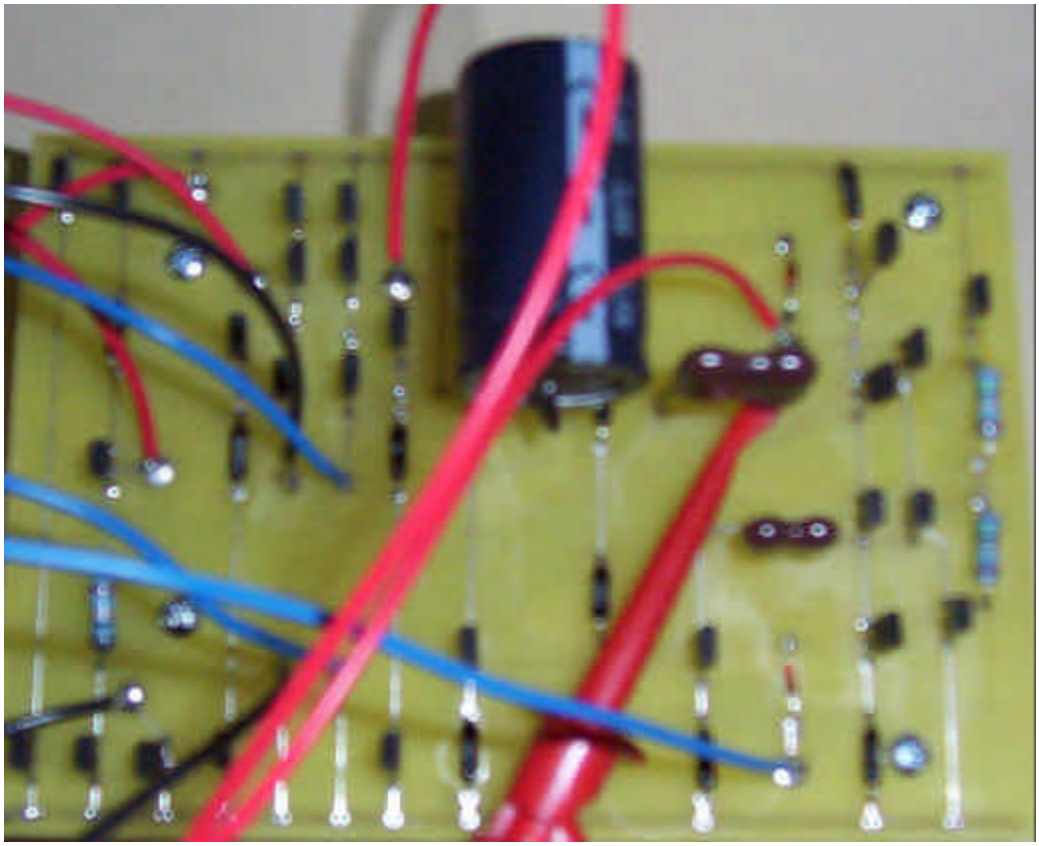


Figure D-1: Populated PCB

Figure D-2: Power Supply

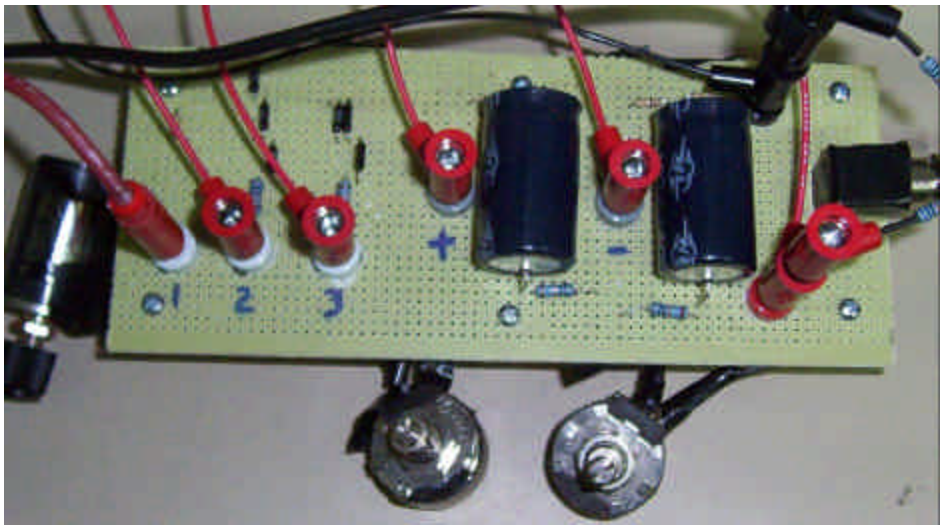


Figure D-3: Test/Biasing Board

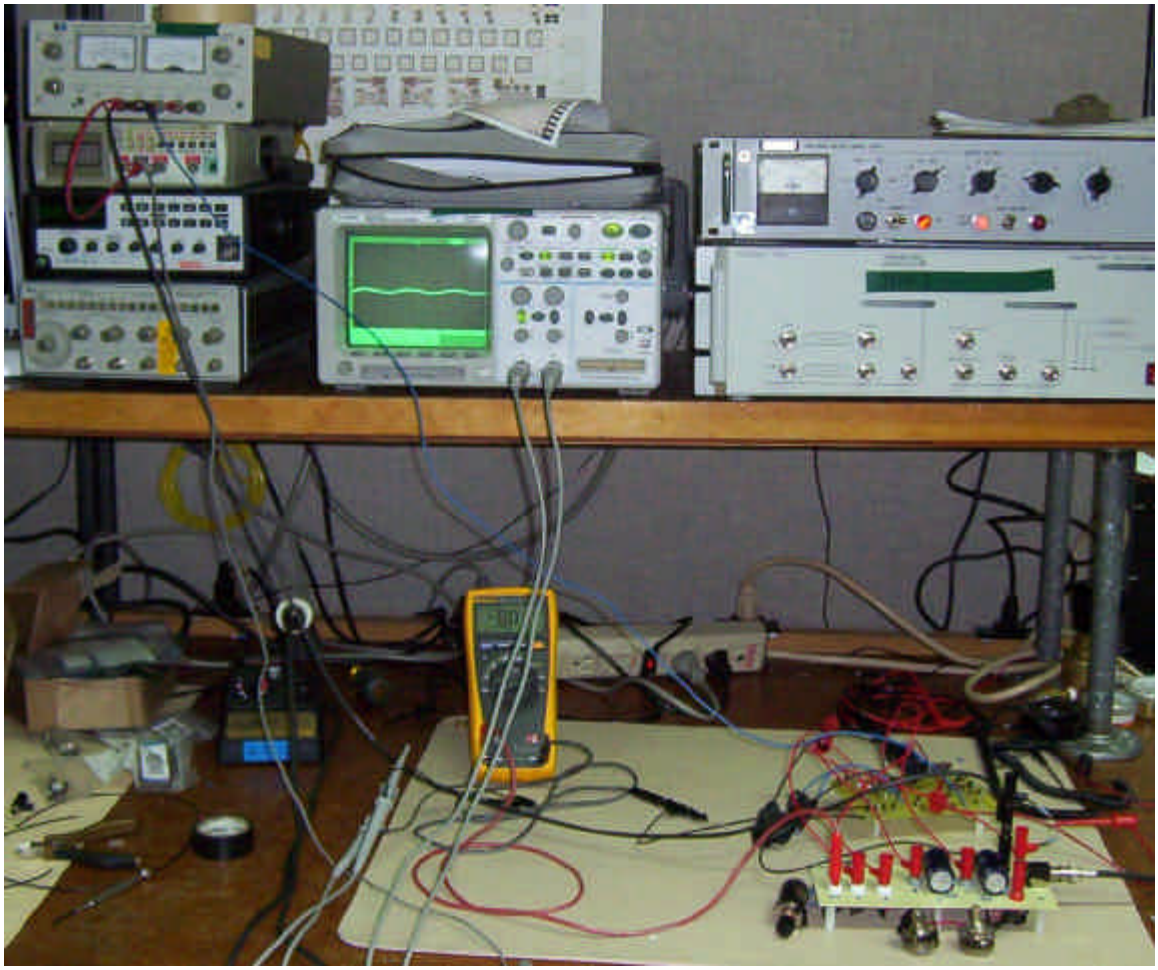


Figure D-4: Test Setup