Main Components

Transmitting/Receiving Nodes:
Four Xilinx Spartan IIE FPGAs

Serializer/Deserializers:
Four National DS92LV16

LVDS Crossbar:
One National SCAN90CP02

Power Supply:
+12V Power Input
Twelve Datel LSN DC/DC Converters
Various Decoupling Capacitors

Solution

Low Voltage Differential Signaling (LVDS)
A widely recognized standard which uses differential current direction to represent logic levels. This allows very high speed serial data to be sent through two 100 ohm matched impedance traces, using approx. 8 times less space than parallel signaling.

Pros
• 350mV switching results in fewer power losses
• Differential design creates little noise and rejects outside interference
• Uses only two lines, no matter what the data transfer rate is

Cons
• Matched impedance lines are more difficult to lay out when creating PCB
• Requires that the components used support the standard and may require component changes

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The team would like to thank the following people for their contributions and help:
Dr. Joe Law, Dr. Herb Hess, Greg Klemesrud and John Geidl