Meeting Minutes

Meeting: Pixel Perfect

Date: Wednesday November, 14, 2012, 4:30 p.m. to 5:05 p.m.

Location: VSRG Lab

Head of Meeting: Dr. Touraj Assefi, Team Advisor

Minute Taker: Darren Allen

In Attendance: Dr. Touraj Assefi, Team Advisor
Darren Allen, Wireless Lead
Daniel Mazo, System Lead
Daniel Micheletti, Team Leader
Kyle Swenson, Software Lead

Absent:

1. Review of Previous Minutes

2. Review of Agenda

   • Might have the Tx module but probably not in time for ASIC tapeout
   • Would have worked originally but due to the manufacturing flaws of the chip, we are only getting 1.4 Mb/s instead of the needed 1.99 – 2 Mb/s
   • Backup Plan #1
     ◦ Use three ASIC pins for transceiver (frame_data, column pointer, and row pointer) to FPGA board, buffer, then send to transmitter
   • Backup Plan #2
     ◦ If problems with ASIC pins, tie FPGA board into pins to USB for PC
   • Backup Plan #3
     ◦ If ASIC does not work, use FPGA board like current design
   • Revamp SPI module so it is simple and potentially pull from FTDI chip if Backup Plan #2 is needed.

3. Summary of Action

   • Continue to work on Tx module

4. Questions